

Class	Subclass	ISSUE CLASSIFICATION

U.S. **UTILITY** Patent Application

**O.I.P.E.**

PATENT DATE

SCANNED

## Q.A

## APPLICANTS

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### Этапы

Field effect transistor with reduced gate delay and method of fabricating the same

PTO-2040  
12/89

ISSUING CLASSIFICATION												
ORIGINAL				CROSS REFERENCE(S)								
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
INTERNATIONAL CLASSIFICATION												

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<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>		<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
___ The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		<b>NOTICE OF ALLOWANCE MAILED</b>  	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____  _____ _____	_____ (Primary Examiner) (Date)		<b>ISSUE FEE</b>	
			Amount Due	Date Paid
___ The terminal ___ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)		<b>ISSUE BATCH NUMBER</b>	
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